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(54) Abstract Title
Temperature-insensitive adjustable CMOS fine delay circuit

(57) A digitally adjustable CMOS fine delay circuit uses the capacitance between the gate and the source/drain of a number of binarily scaled NMOS transistors N0-N5. The capacitance of each transistor is dependent on the digital signal applied to its gate so that a digitally selectable capacitance is produced in dependence on the signals D(0)-D(5). The charging resistor 31 is of polycrystalline construction, which improves temperature insensitivity.

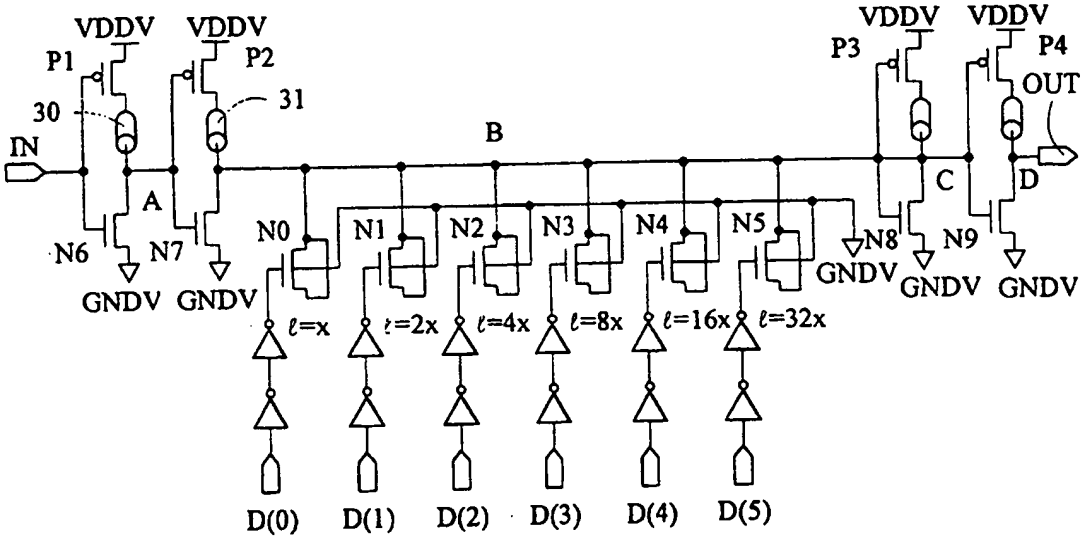

Fig. 3

$Z = \frac{1}{jwC}$

$C \to 0$

$Z \to \infty$

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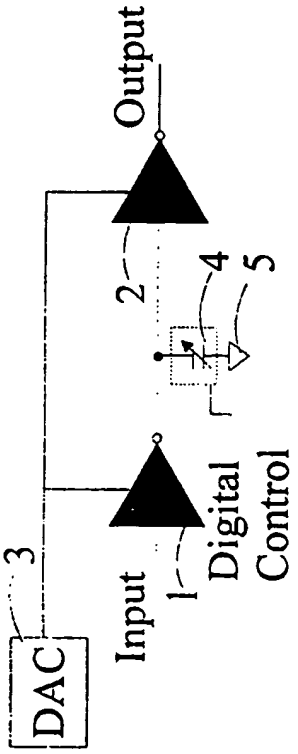


Fig. 1

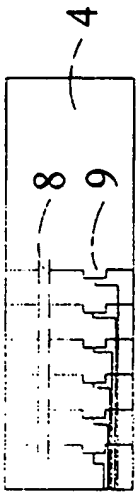


Fig. 1b

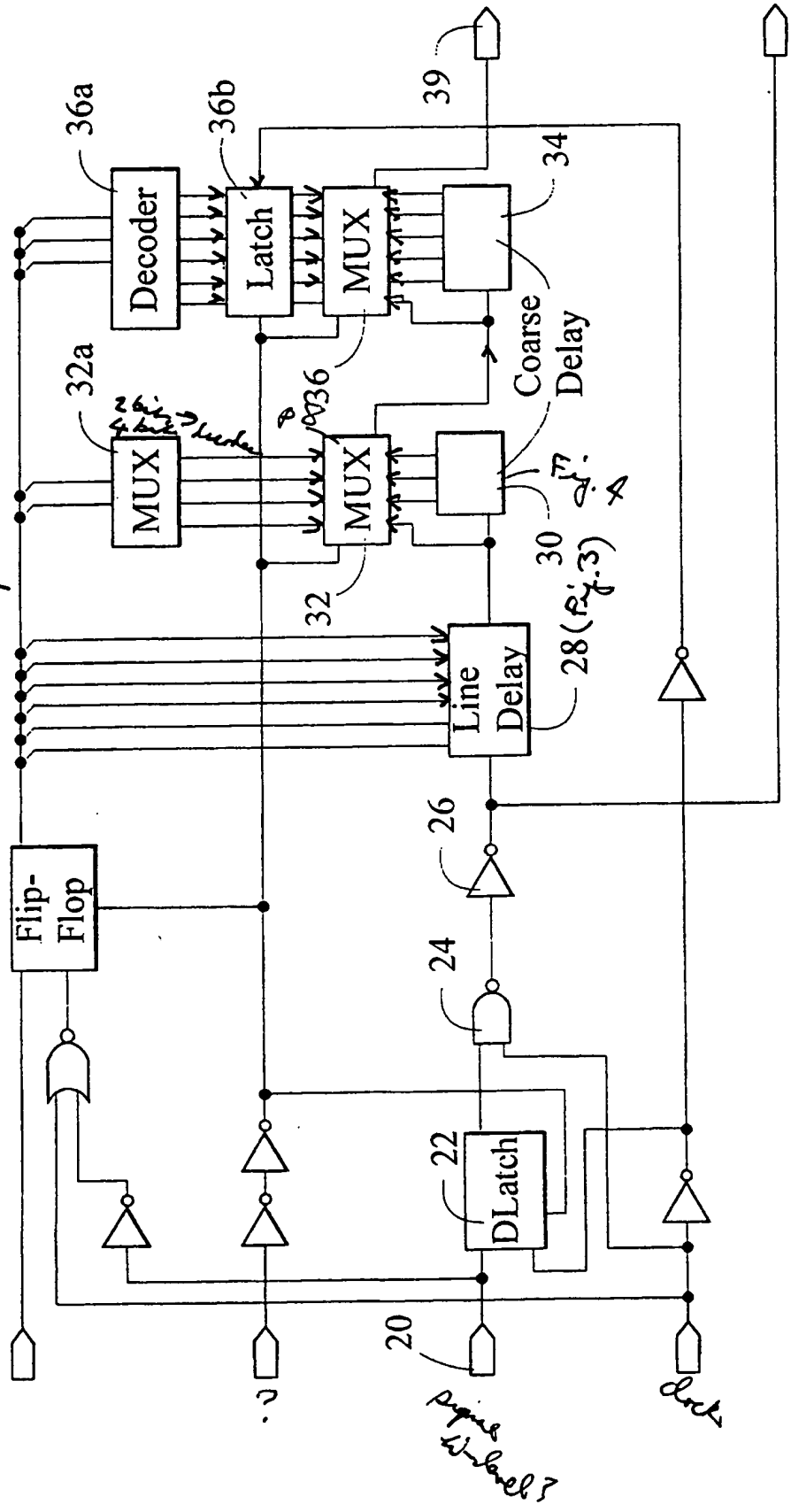

Decoder
Latch
MUX
MUX
MUX
Coarse Delay
Line Delay
Flip-Flop
DLatch
36a
36b
32a
32
34
30
28
26
24
22
20
39

Fig. 2

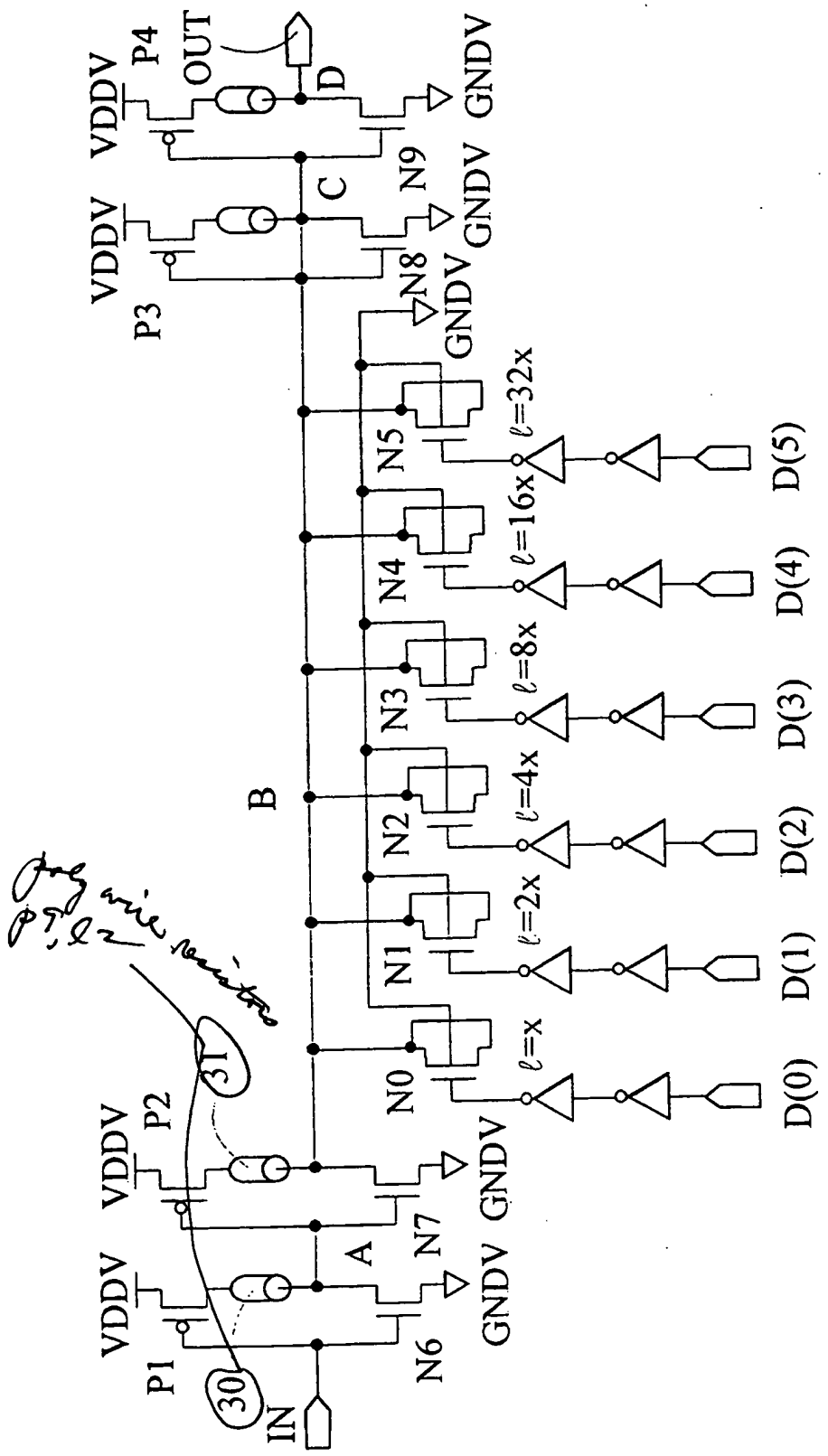

VDDV
P4
OUT
D
GNDV
VDDV
C
N9
GNDV
VDDV
P3
N8
GNDV
N5
ℓ=32x
N4
ℓ=16x
B
N3
ℓ=8x
N2
ℓ=4x
N1
ℓ=2x
N0
ℓ=x
D(5)
D(4)
D(3)
D(2)
D(1)
D(0)
VDDV
P2
3T
VDDV
A
N7
GNDV
GNDV
VDDV
P1
30
IN
N6

Fig. 3

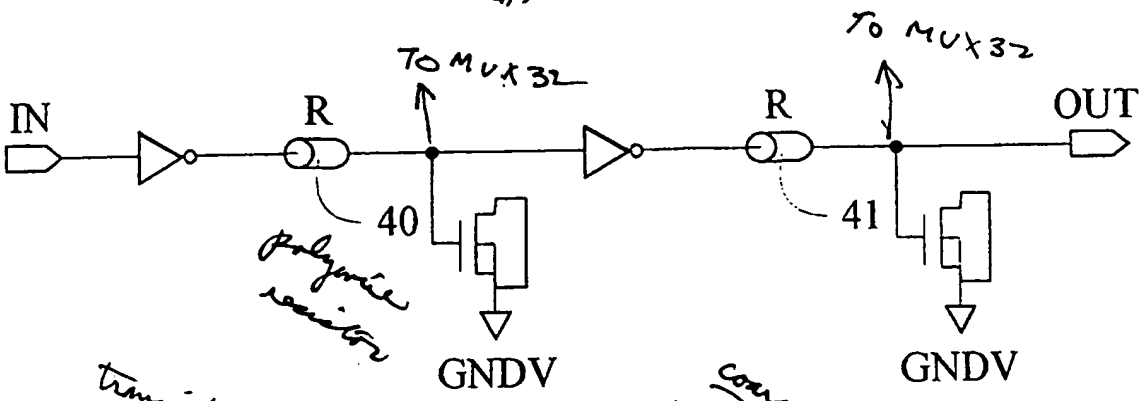


Fig. 4

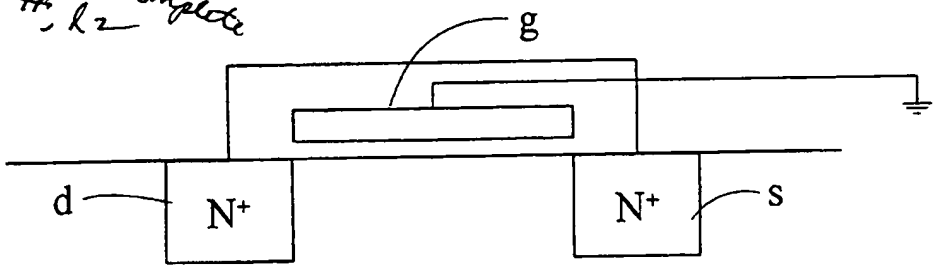


Fig. 5a

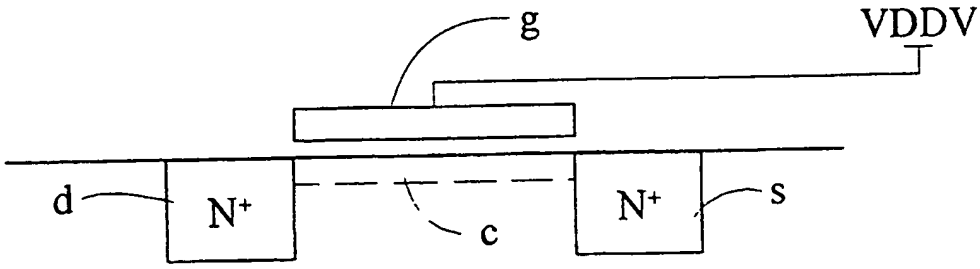


Fig. 5b

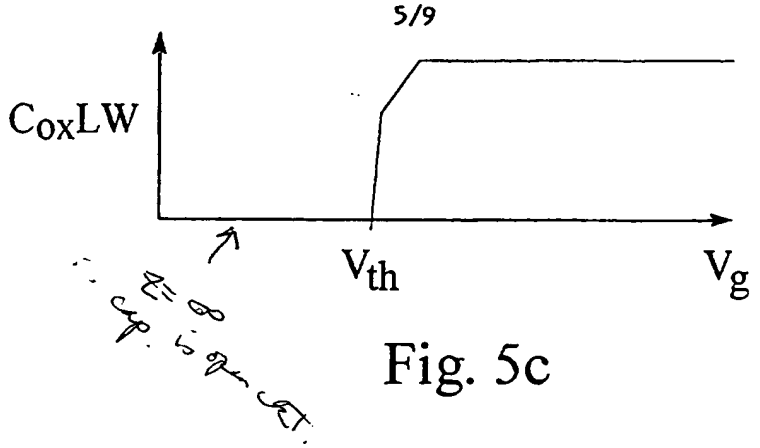


Fig. 5c

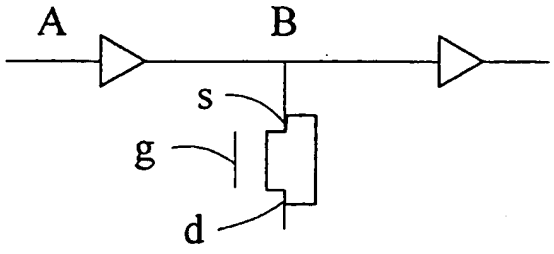


Fig. 6a

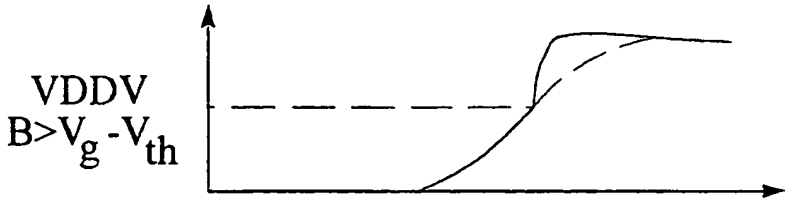


Fig. 6b

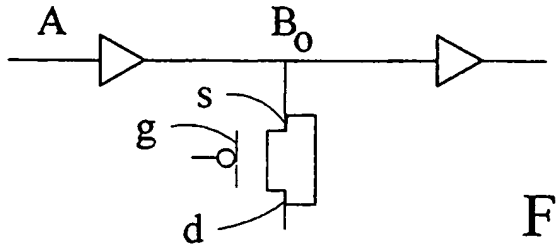


Fig. 7a

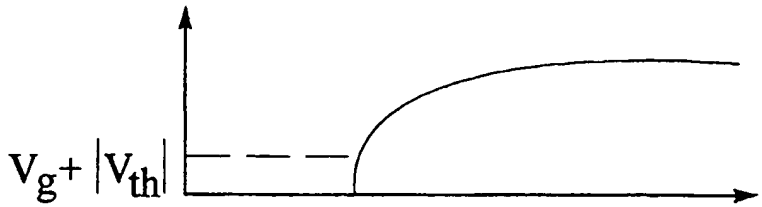


Fig. 7b

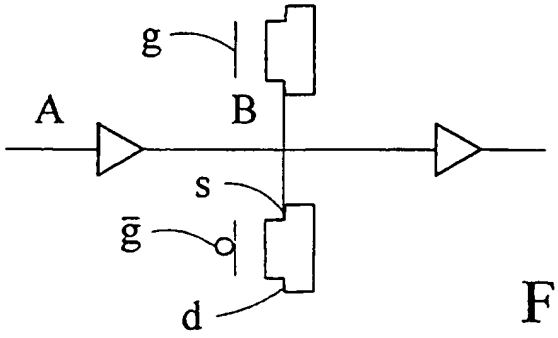


Fig. 8a

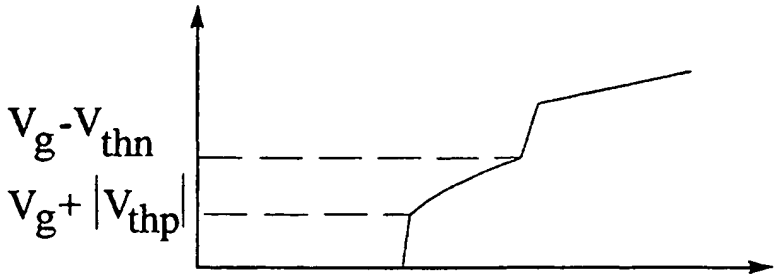


Fig. 8b

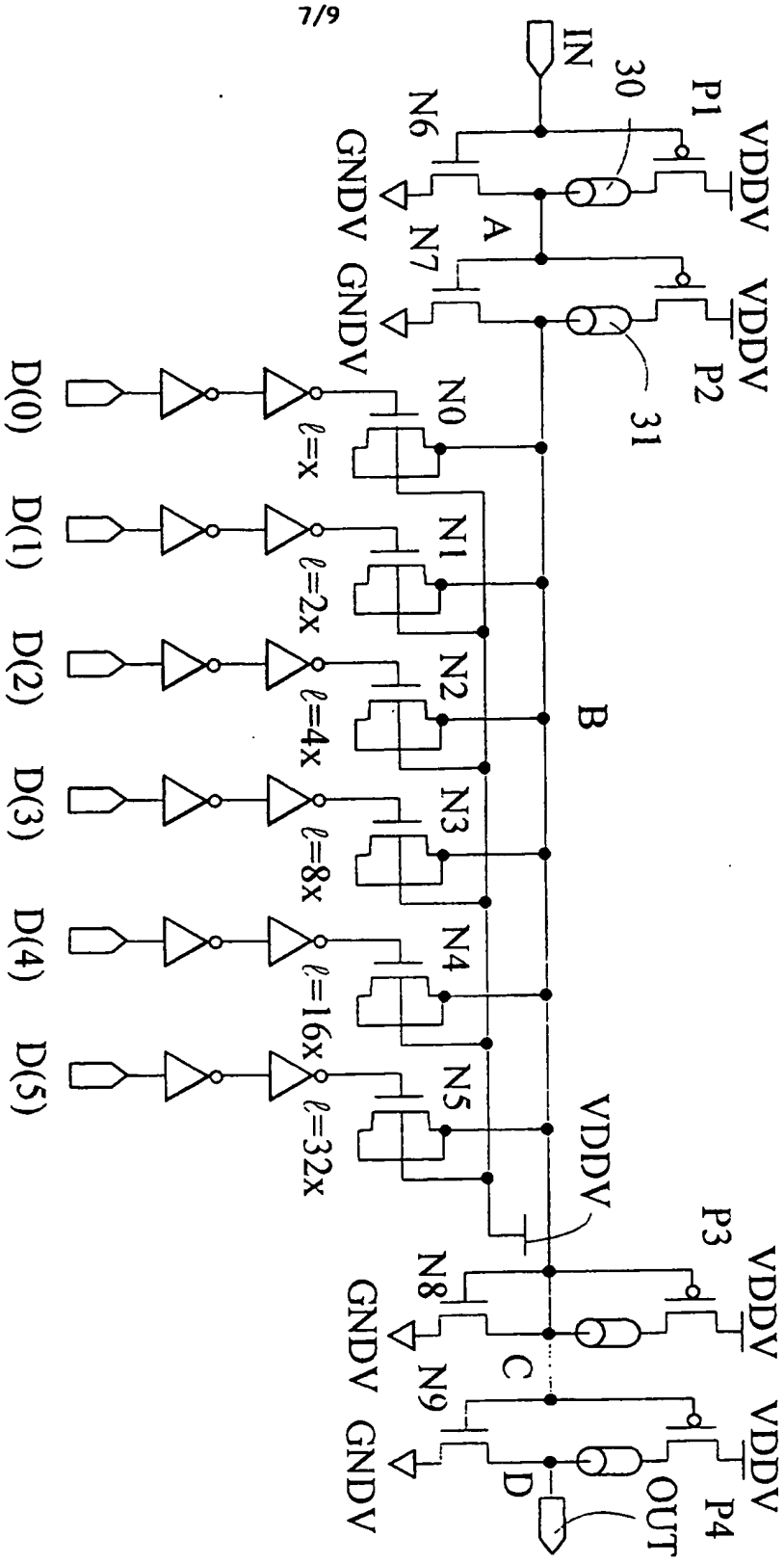
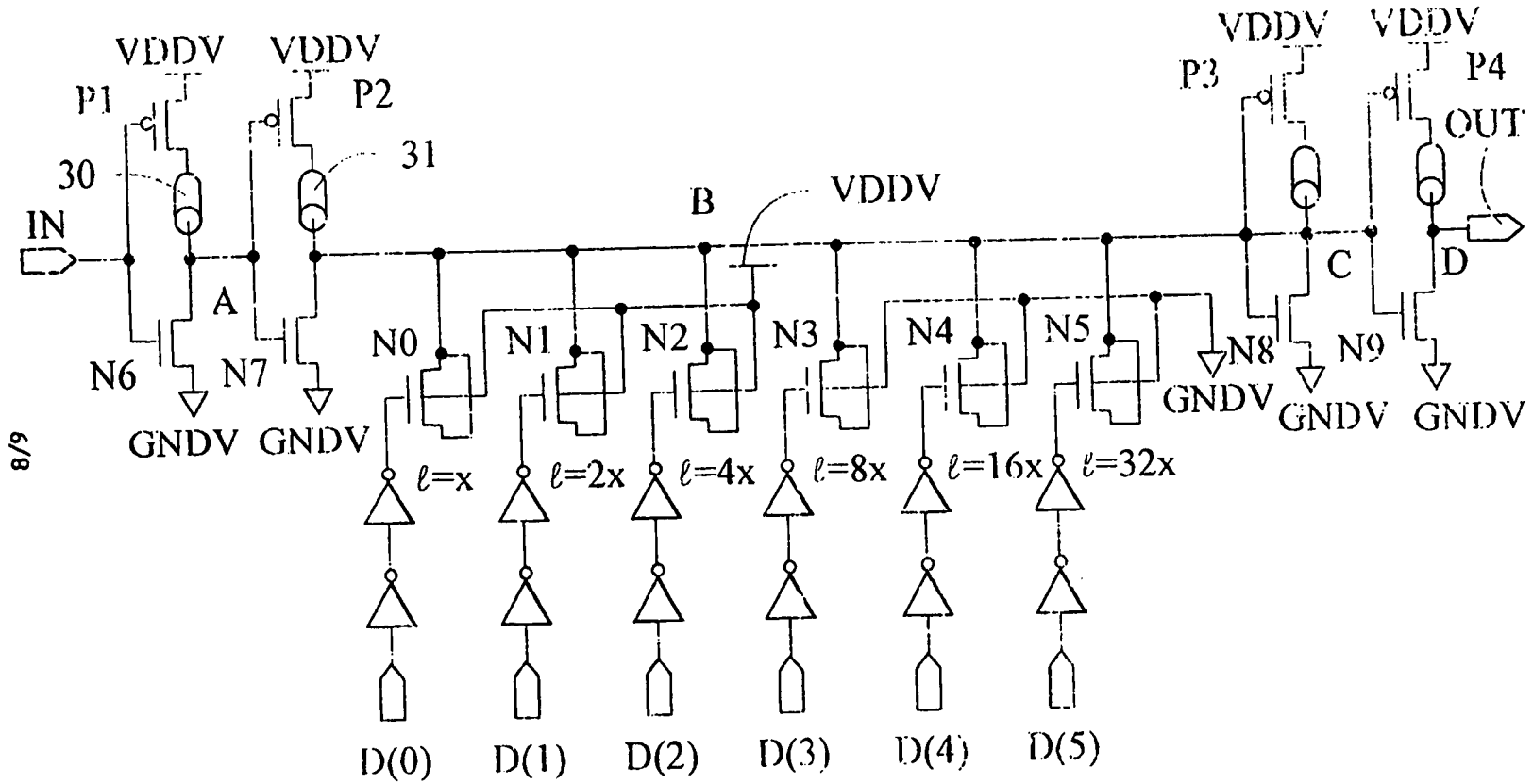

IN
30
P1
VDDV
N6
GNDV
A
N7
GNDV
VDDV
P2
31
N0
N1
N2
N3
N4
N5
B
VDDV
P3
VDDV
N8
GNDV
C
N9
GNDV
VDDV
P4
OUT
D
ℓ=x
ℓ=2x
ℓ=4x
ℓ=8x
ℓ=16x
ℓ=32x
D(0)
D(1)
D(2)
D(3)
D(4)
D(5)

Fig. 9


VDDV
VDDV
P1
P2
30
31
IN
A
B
VDDV
VDDV
VDDV
P3
P4
OUT
C
D
N6
N7
N0
N1
N2
N3
N4
N5
N8
N9
GNDV
GNDV
GNDV
GNDV
GNDV
GNDV
ℓ=x
ℓ=2x
ℓ=4x
ℓ=8x
ℓ=16x
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D(0)
D(1)
D(2)
D(3)
D(4)
D(5)
8/9

Fig. 10

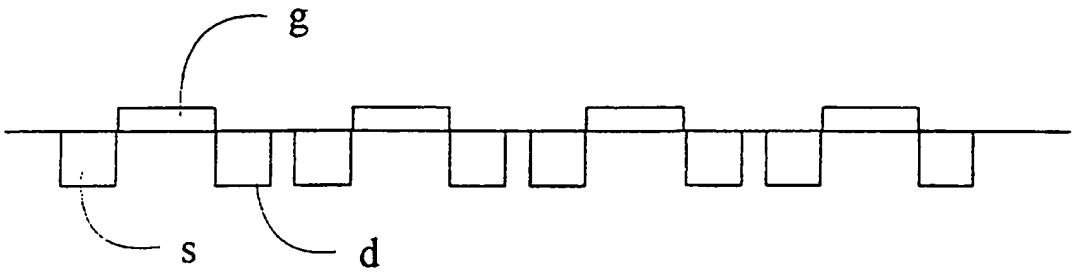

Fig. 11

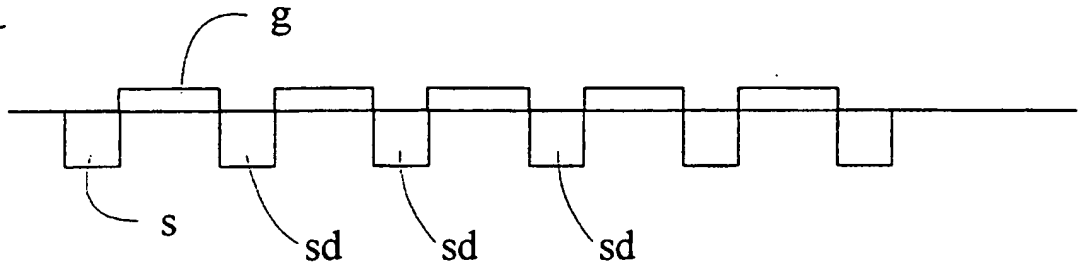

Fig. 12a

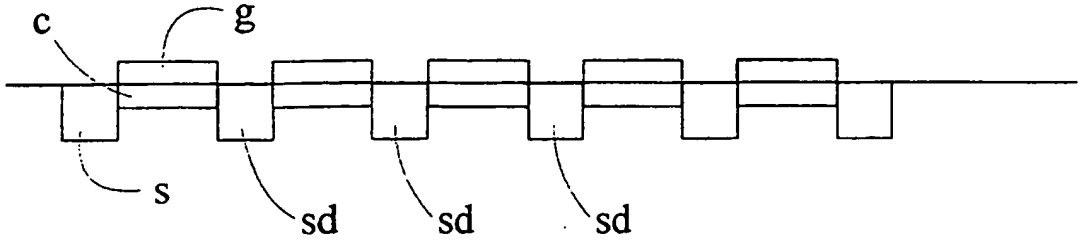

Fig. 12b

Delay Circuits

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Field of the Invention

This invention relates generally to delay circuits, e.g. CMOS delay circuits, and more particularly to a vernier delay circuit with digitally switchable capacitors providing varying delay.

Background of the Invention

CMOS circuit design for low power and inexpensive integrated circuits is well known. Many common integrated circuit products are available in CMOS implementations. Unfortunately, the low power consumption of CMOS circuits is achieved at a cost. CMOS integrated circuits are very susceptible to temperature and electrical variations. The inherent delays in CMOS integrated circuits are substantial and vary significantly with temperature and other variations. Because of this, CMOS timing and delay circuits are difficult to design.

Prior Art

Test systems require accurate calibration and de-skewing of timing parameters. Programmable delay circuits, also referred to as programmable delay lines, are ideal for providing necessary calibration and de-skewing, as they allow for customised timing delays. The delays are then applied at each test. Alternatively, different delays are provided at each test. With the increase in clock speeds for circuits, test circuits must accurately test at higher speeds. Increased clock speed of a tester translates to increased precision for a delay circuit. Coarse delay lines comprised of inverters, RC circuits, and multiplexers can not produce the required precision; a higher resolution delay circuit is required.

A typical fine delay line is implemented using a combination of serial and parallel paths of loaded inverters. The resolution of the delay line is thereby increased. Unfortunately, such a circuit is bulky and varies significantly with changes in temperature.

Another method of implementing a high resolution delay circuit uses a vernier delay circuit. A typical vernier delay component is the Brooktree® Bt604. The component is an ECL compatible implementation of a vernier delay circuit comprising a digital to analogue converter (DAC), a latch, a linear ramp generator, and a comparator. Digital input in the form of a multiple bit signal to the DAC is converted to one of a plurality of analogue voltages. A constant current source charges a capacitor and thereby forms a linear ramp response. When charge on the capacitor exceeds the analogue voltage provided by the DAC, the output is provided. Setting the analogue voltage is achieved by varying the data bits provided to the DAC. A latch holds data for output during the delay. As a single current is selected to charge the capacitor, the capacitor charges in a linear fashion and therefore, delays are accurate. Minimum and maximum delays are dependent upon the voltage range over which the capacitor is charged; however, the linear nature of the response allows for a considerable degree of flexibility. The use of bipolar technology makes the circuit relatively immune to temperature variations; however, the circuit consumes a significant amount of power.

The Bt604 is an very good timing delay component. Unfortunately, it requires an external current reference source for accurate delays. Further, the Bt604 is a separate hardware component occupying board space and increasing design costs. Incorporating the circuit of the Bt604 into a CMOS device requires significant changes to redesign the bipolar circuit as a CMOS circuit.

In United States Patent 5,280,195, Goto et al. disclose a timing generator. The timing generator comprises a timing vernier. The coarse delay timing circuit provides a plurality of delay paths that are distinct in order to more effectively produce desired timing delays. The fine delay timing circuit of the timing vernier used in the implementation described by Goto et al. is not disclosed in detail and is prior art to the disclosure.

Prior art switchable capacitors are known. Some examples of switchable capacitors are disclosed in united States Patent 5,332,997 to Dingwall, et. al. Issued July

26, 1994. Dingwall discloses a capacitor in series with a switching transistor for turning the capacitor "on" or "off." In United States Patent 5,495,199 to Hirano and issued Feb. 27, 1996, a similar switched capacitor is disclosed.

In an article entitled, "CMOS Programmable Delay Vernier," Hewlett Packard Journal Vol. 45, No. 5, Oct 1994 pp.51-58 by Goto, Barnes, and Owens disclose a CMOS implementation of a delay vernier. The implementation disclosed relies on prior art digitally controlled RC circuits. An example of known digitally controlled RC circuits is transistors in series with capacitors, and buffer impedance occurring naturally within CMOS logic to form a variable RC circuit. A DAC is used to provide a bias voltage to reduce the effects of temperature, layout, and process variations. The use of a bias voltage provided by a DAC may compensate for temperature variations, but is complex and requires significant space on a CMOS integrated circuit.

It would be advantageous to provide a simple and relatively temperature invariant vernier timing delay for implementation in CMOS integrated circuits.

Object of the Invention

In an attempt to overcome these and other limitations of the prior art, it is an object of the present invention to provide a CMOS delay circuit that is substantially temperature invariant.

It is a further object of the invention to provide a CMOS vernier delay that makes efficient use of CMOS integrated circuit area.

Statement of the Invention

In accordance with the invention there is provided a CMOS variable delay circuit comprising:

a) an input terminal;

b) an output terminal;

c) a reference voltage terminal;

d) a resistive means coupled in series with the input terminal and the output terminal;
e) a transistor having a source, a gate, a drain, and a substrate, the source and the drain electrically coupled with at least one of the output terminal, and the resistive means, and the substrate electrically coupled with the reference voltage terminal; and
f) means for providing to the gate a digital signal having at least two voltage levels for selecting from a plurality of gate-channel capacitances.

In accordance with the invention there is further provided a CMOS variable delay circuit comprising:
a) an input terminal;
b) an output terminal;
c) a first reference voltage terminal;
d) a second reference voltage terminal;
e) a resistive means coupled in series with the input terminal and the output terminal;
f) a plurality of n-type transistors having a source, a gate, a drain, and a substrate, the source and the drain electrically coupled with at least one of the output terminal, and the resistive means, and the substrate electrically coupled with the first reference voltage terminal;
g) a plurality of p-type transistors having a source, a gate, a drain, and a substrate, the source and the drain electrically coupled with one of the input terminal, the output terminal, and the resistive means, and the substrate electrically coupled with the second reference voltage terminal;
h) means for providing to each gate a digital signal having at least two voltage levels for selecting from a plurality of gate-channel capacitances.

In accordance with a further aspect of the invention there is provided a fine delay circuit for use in a vernier delay circuit comprising:

a) an input terminal;

b) an input buffer comprising at least a first transistor comprising a first gate coupled with the input terminal, a first source coupled with a voltage terminal V_{DD}

and a first drain, and a poly resistor having a first terminal and a second terminal, the first terminal electrically coupled with the first drain;

c) an output terminal electrically coupled to the second terminal of the poly resistor;

d) a first reference voltage terminal,

e) at least a second transistor having a second source, a second gate, a second drain, and a substrate, the second source and the second drain electrically coupled with at least the output terminal, and the substrate electrically coupled with the first reference voltage terminal; and,

f) means for providing to the second gate a binary digital signal for selecting between a first gate-channel capacitance and a second substantially higher gate-channel capacitance.

An advantage of the present invention is an elimination of complex feedback and control circuitry from a CMOS vernier delay.

A further advantage of the invention is the reduction in intrinsic delay of a vernier delay circuit.

Brief Description of the Drawings

Exemplary embodiments of the invention will now be described in conjunction with the following drawings, in which:

Fig. 1 is a simplified diagram of a prior art embodiment of a fine delay element for use in a CMOS implementation of a vernier delay circuit;

Fig. 1b is a schematic diagram of a prior art variable capacitor for use in the circuit of Fig. 1;

Fig. 2 is a high level schematic diagram of a vernier delay circuit according to the invention;

Fig. 3 is a detailed schematic diagram of a fine delay circuit for use in the circuit of Fig. 2 and according to the invention;

Fig. 4. is a detailed schematic diagram of a delay circuit having a substantially fixed delay;

Fig. 5a is a simplified diagram of an NMOS transistor with a low voltage applied to the gate;

Fig. 5b is a simplified diagram of an NMOS transistor with a high voltage applied to the gate;

Fig. 5c is a graph illustrating the capacitance of the transistor shown in Figs. 5a and 5b;

Fig. 6a is a schematic diagram of a delay circuit comprising an NMOS transistor;

Fig. 6b is a graph of voltage at B in the circuit of Fig. 6a;

Fig. 7a is a schematic diagram of a delay circuit comprising a PMOS transistor;

Fig. 7b is a graph of voltage at B in the circuit of Fig. 7a;

Fig. 8a is a schematic diagram of a delay circuit comprising an NMOS transistor and a PMOS transistor;

Fig. 8b is a graph of voltage at B in the circuit of Fig. 8a;

Fig. 9 is a detailed schematic diagram of a fine delay circuit using PMOS transistors and according to the invention;

Fig. 10 is a detailed schematic diagram of a fine delay circuit using NMOS transistors and PMOS transistors and according to the invention; and,

Fig. 11 is a simplified layout diagram for laying out transistors in a fine delay element according to the prior art;

Fig. 12a is a simplified layout diagram for laying out transistors in a fine delay element according to the invention; and,

Fig. 12b is a simplified layout diagram for laying out transistors in a fine delay element with induced channels shown in dashed line according to the invention.

Detailed Description

A vernier delay circuit is generally known. In a common implementation of a vernier delay circuit, a course delay and a fine delay are implemented using RC circuits. The delays are often switchable allowing for modification of delay times. Delay tuning is achieved by calibrating the circuit to set a delay at a desirable level and operating the

calibrated circuit until further calibration is performed. Alternatively, delay timing is changed periodically.

Referring to Fig. 1, a prior art circuit diagram for a fine tuning delay circuit of a vernier delay and for use in CMOS is shown. An input buffer **1** is provided with an input signal at an input thereof. The buffered signal is provided from an output of the input buffer **1** to an input of an output buffer **2**. The output of the output buffer **2** forms the circuit output. A variable capacitor **4** is coupled between ground **5** and the output of the input buffer **1**. The buffered signal charges the variable capacitor **4**. The resistance in the output of the input buffer **1** and in the input of the output buffer **2** combined with the capacitance of the variable capacitor **4**, forms an RC circuit. This results in a signal delay dependent upon the intrinsic resistance and the capacitance.

A DAC **3** provides a biasing voltage to the buffers **1** and **2** in order to calibrate the vernier delay and in order to compensate for temperature variations. The use of a DAC for this purpose is well known. The biasing voltage is necessary to compensate for variations in the resistance in the output of the input buffer **1** and in the input of the output buffer **2**; variations in resistance result in undesirable changes to the value of RC.

Referring to Fig. 1b, a prior art variable capacitor is shown. A capacitor **8** is connected in series with a transistor **9**. The series capacitor **8** and transistor **9** are in parallel with other series capacitors and transistors. A digital input signal is provided to each transistor gate. When a signal is sufficient to turn a transistor "on," a series capacitor associated with the transistor forms part of the RC circuit. When a transistor is "off," an associated series capacitor does not charge and, therefore, does not form part of the RC circuit. This is a simplified explanation of the circuit of Fig. 2. A more detailed analysis of the circuit is not necessary for an understanding of the present invention.

Referring to Fig. 2, a block detailed schematic of a vernier delay circuit for implementation in CMOS according to the present invention is shown. An input signal is provided at an input port **20**. The input signal is provided to a D latch **22**. From the D

latch **22**, a signal is gated with a clock signal in a logic gate **24** in the form of a NAND gate and provided to an input buffer **26** and then to a fine delay circuit **28**.

A plurality of digital input signals D(10:0) are provided to a series of flip flops **27** for holding the signals during an appropriate interval. Once set or cleared, a plurality of the digital input signals in the form of D(5:0) are provided to the fine delay circuit **28** for control of delay timing. These signals are shown forming part of a data bus. From the fine delay circuit **28** the delayed signal is provided to a first coarse delay circuit **30**. The first coarse delay circuit **30** delays the signal provided thereto by 3 different time delays - a delay of 550ps, a delay of 1100ps, and a delay of 1650ps. A multiplexer **32** receives the signal provided to the first coarse delay circuit **30** and the three differently delayed signals and in dependence upon signals from the data bus D that have been decoded in a two bit to four bit decoder **32a**, provides one of the four decoder outputs to a second coarse delay circuit **34**. The second coarse circuit **34** delays the signal provided thereto by 5 different delays in the form of n x (m x 550ps), where n is 1 to 5 and m is a predetermined coarseness for the delay of, for example, 4. The second set of delayed signals are provided to a multiplexer **36** along with the signal provided to the second coarse delay circuit **34**. In dependence upon signals from the data bus D that have been decoded in a three bit to six bit decoder **36a** and latched in latch **36b**, provides one of the seven signals a circuit output port **39**.

The input signal received at the input port **20** is thereby delayed by three separate circuits a first fine delay circuit **28**, a first coarse delay circuit **30**, and a second coarse delay circuit **34**. It will be apparent to those of skill in the art that this need not be so. Optionally, any number of fine and coarse delay elements are used. It is further known that increasing the number of circuits or rearranging their order may vary timing by altering latching, changing intrinsic delays, varying inter element interference, and other design considerations.

Figs. 3 and 4 are detailed schematic diagrams of high level blocks shown in Fig. 2. Referring to Fig. 3, a detailed schematic diagram of the fine delay element **28** is shown.

A signal provided to the fine delay element **28** is buffered through P1 and N6 and then again through P2 and N7. Poly wire resistors **30** and **31** provide a substantial portion of resistance for an RC circuit. The use of poly wire resistors in series with CMOS inverters improves temperature invariance of the overall resistance as poly wire resistors are less temperature sensitive than intrinsic CMOS buffer output resistance i.e. an inverter without a resistor in series therewith. Resistor values for resistors **30** and **31** are selected to be significantly larger than the intrinsic impedance of the transistors P1, P2, N6, and N7. The buffered signal B is provided to an output buffer comprising four transistors P3, P4, N8, and N9. The buffered signal B is also provided to a source and a drain of each NMOS transistor N0 - N5. Transistor substrates for transistors N0-N5 are electrically connected to ground. A capacitor is formed between the gate oxide and an induced channel of each transistor. The formed capacitors are disposed in parallel. As is well known in the art of electronics, capacitors disposed in parallel are modelled by adding their capacitances together.

The capacitors N0-N5 are each formed of an NMOS transistor having a source and drain shorted together and having a substrate connected to ground. A gate of each transistor is provided a data signal from the data bus, shown here as D(5:0). The data signals D(5:0) are each electrically coupled to a gate of a transistor. Each NMOS transistor N0 - N5, has a different capacitive value. A large degree of flexibility is supported when exponentially increasing values in the form of n, 2n, 4n, 8n, 16n, and 32n are selected and where n corresponds to a capacitance required to produce a delay of the desired resolution of the fine delay circuit.

Referring to Fig. 5a, a simplified diagram of an NMOS transistor is shown. A gate g is spaced from a drain d and a source s in a conventional manner. The source s and drain d are situated in a P type substrate and electrically coupled. Between the gate g and the source s there exists an intrinsic capacitance. This capacitance is very small both due to distance and due to surface area of the capacitive plates in the form of the source and the gate. In Fig. 5a, the gate is shown coupled to ground or another low voltage source. In

this state the intrinsic capacitance is substantially the intrinsic capacitance of the transistor which is substantially negligible.

Referring to Fig. 5b, the transistor of Fig. 5a is shown wherein the gate g is connected to a voltage high source. A voltage high source is conventionally 5 volts but may vary over known and well-understood ranges. When a voltage is applied to the gate g, a channel c forms between the source s and the drain d. This allows a conventional transistor to operate as a switch. As is evident from Fig. 5b, the channel c and the gate have a substantially increased capacitance; the separating distance between capacitor plates is reduced and their surface area is increased over those of Fig. 5a. Here, the capacitance is approximated by $C_{gds} = C_{ox} W L$; where W L is effectively the area of the capacitive plates and more specifically the dimensions of the gate.

Referring to Fig. 5c, a graph of the capacitance of an NMOS transistor as shown in Figs. 5a and 5b is shown. The capacitance is substantially 0 until a threshold voltage V_{th} is applied to the gate g. At this voltage, a channel c is formed and the capacitance rises sharply to the value approximated by the equation above. More detailed analysis is present in Appendix A.

In operation as a digitally controlled capacitor, PMOS and NMOS transistors are not identical. Referring to Fig. 6a, a simplified circuit diagram of a digitally controlled capacitor as described above is shown. An input terminal A receives an input signal and provides same to an input buffer. The output of the input buffer B is connected to a digitally controlled capacitor. Since voltages are relative, when the voltage at B, V_{sd}, rises above the voltage at the gate minus V_{th} the capacitance is substantially 0. The capacitance follows the curve of the graph shown in Fig. 5c where V_g is replaced by $V_g - V_{sd}$.

For rising edge delay, the NMOS transistor described above allows the voltage at B to follow a rise similar to that set out in Fig. 6b. A standard curve for charging a capacitor in an RC circuit is shown in dashed line. As can be seen from the graph, when

$V_g - V_{th}$ is less than V_B, the capacitor turns off and the voltage at B rises sharply. This is desirable as a sharper rising edge results.

Referring to Fig. 7a, a simplified circuit diagram of a digitally controlled PMOS capacitor is shown. An input terminal receives an input signal and provides same to an input buffer. The output of the input buffer B_o is connected to a digitally controlled PMOS capacitor. Referring to Fig. 7b, a graph of the response at B_o to a rising edge while the PMOS transistor is operating as a capacitor is shown. Here the sharp rise occurs initially and then a substantially standard capacitor charging curve for an RC circuit is followed. The fast initial voltage increase and the rounded signal in place of a squared signal are less desirable. Conversely, PMOS is better suited to falling edge delays as the rapid voltage drop occurs once V_g drops below V_{th}.

Referring to Fig. 8a, a circuit comprising an NMOS digitally controlled capacitor and a PMOS digitally controlled capacitor is shown. In Fig. 8b, a graph of the response at B to a rising edge is shown. A reversed but similar graph applies to the falling edge. Using both NMOS and PMOS transistors in this fashion allows delay of both rising and falling edges while maintaining many of the benefits of each.

The source/drain-to-gate capacitance C_{g-d} of an NMOS transistor changes from 0 to a known capacitance when V_g changes from low to high, i.e. the capacitance is programmable via the gate voltage V_g. The source/drain-to-gate capacitance C_{g-d} of PMOS transistor changes from 0 to a known capacitance when V_g changes from high to low. This programmable capacitance approach is used to control the delay in the CMOS vernier which results in a delay circuit which is less sensitive to the temperature, is simple to construct, and whose inherent delay is significantly reduced. At any time, a capacitance of the sum of the capacitances of each transistor exists between B and ground. This capacitance is modified by modifying D(5:0) to change the state of each transistor acting as a capacitor from "on" to "off" or from "off" to "on."

The whole delay of the circuit shown in Fig. 3 is a summation of delays through the input buffer, through the output buffer and at node B itself. The buffer delays are

modelled as intrinsic delay; the delay formed by the poly resistors and the digitally controlled capacitors forms a variable delay.

For a single transistor as described above, the gate-channel capacitance is approximated by $D(i)(C_{ox}W_iL_{eff-i})$, where D(i) is a 0 or a 1 in dependence upon a voltage applied to the gate of the transistor, W and L_{eff} are dimensions of the gate, and i is a transistor identifier. Referring to Fig. 3, when 6 transistors are present and identified as 0-5, the total capacitance is

$$C_b = \sum_0^5 c_{ox} W_i L_{eff-i} D(i) + C_L$$

By selecting exponentially increasing values for WL as set out above wherein $W_iL_{eff-i} = \frac{1}{2}W_{i+1}L_{eff-i+1}$, thereby doubling the effective gate area from one transistor to the next, the above equation is solved as

$$C_b = c_{ox} W_0 L_{eff-0} \sum_0^5 2^i D(i) + C_L .$$

This equation reduces to C_L when all D(i) are 0, and allows for considerable flexibility in the value of the summation. Clearly, the capacitance C_b is programmable through a series of binary input signals.

The minimal capacitance is considered negligible and throughout this disclosure is approximated by 0 capacitance; this is not truly so. During design, the minimal capacitance is modelled in order to establish intrinsic delay of the fine delay circuit **28**. In this respect, it is a design decision balancing intrinsic delay with flexibility that determines a number of transistors used as capacitors in the fine delay circuit **28**. Further, each transistor is designed to support a substantial difference in capacitance between an "on" state and an "off" state.

It will be obvious to those of skill in the art that a variation in temperature affects the circuit delay as described herein. The delay is related to RC. C is formed of an

intrinsic capacitance and a variable capacitance. R is formed of an intrinsic resistance and the resistance of the poly wire resistors. Therefore, (Ri + Rpw)(Ci + Cv) is related to the delay. Ci and Cv vary little with temperature in the above design. Rpw is known to vary little with temperature. Ri varies considerably with temperature. When Rpw is selected as substantially larger than the variation in Ri over a predetermined range of temperatures, the variation in the delay timing is maintained within predetermined limits. In the above design Rpw is approximately 10 times Ri, this has been found to be suitable in a present application. Other applications may require a higher value or allow a lower value of Rpw relative to Ri. Alternatively, in some temperature controlled environments, Rpw is not necessary.

Alternatively, a different buffer circuit from that shown in the figures is employed in the circuit. Alternatively, other temperature compensation means in place of the poly wire resistors is used. Examples of temperature compensation means include temperature control in the form of heating or air conditioning, internal IC heating and temperature maintenance, etc. Alternatively, a voltage that swings with temperature is used as an input signal to a DAC in order to program a further delay circuit in dependence upon temperature fluctuations. Further alternatively, the capacitors are connected between **B** and a second level other than ground, for example, for a delay circuit having a different device type or rest state than those disclosed herein. Capacitance between **B** and a voltage source in the form of VDD allows an opposite polarity to be supported.

Further alternatively, p type and n type transistors are used in a single fine timing delay circuit **28** to delay rising and falling edges as described above.

The use of transistors to form digitally controlled capacitors, results in a smaller number of components for the fine delay circuit **28**. A smaller number of components is usually accompanied by lower intrinsic delays and a reduction in inter component interference. This is the case in the above described circuit. Of course it will be apparent to those of skill in the art that layout has significant effects upon intrinsic delay and inter component interference and that layout should be undertaken to reduce these effects.

Lower inter component interference often results in higher frequency response and/or better bandwidth.

The use of capacitors in series with transistors for providing variable capacitance as known in the prior art increases integrated circuit area, complicates layout, and increases path lengths, intrinsic delay, and inter component effects. As such, it is advantageous to use digitally controlled capacitors as herein disclosed.

The schematic of Fig. 3 shows NMOS transistors but it will be apparent to those of skill in the art that PMOS transistors will also function as desired. A PMOS implementation and a mixed NMOS PMOS implementation are described with specific reference to Figs. 9 and 10.

Referring to Fig. 4, a detailed schematic of a coarse delay element is shown. As the delays provided by the coarse delay elements are not variable - the delayed signals are switched with a multiplexer - each delay circuit is identical. Alternatively, each delay circuit is similar but not identical. Alternatively, different delays are implemented using different delay elements. For the first coarse delay circuit **30** to produce 3 different delays, a single delay path is used having three delay elements. This is shown in detail in Fig. 6. Each delay element is substantially the same as the circuit shown in Fig. 4. Alternatively, three separate delay paths are used.

Again, referring to Fig. 4, poly wire resistors are used to improve temperature invariance. The delay of the circuit is substantially 550ps. Transistors **43** are used as junction capacitors, as is well known in the art.

The first coarse delay circuit **30** is formed of three delay circuits, as shown in Fig. 4, disposed in series with an output drawn from each of the delay circuits to outputs of the first coarse delay circuit **30**.

Multiplexers are well known in the art and, therefore, the multiplexer will not be discussed further or shown in detailed schematic. Decoders of this type of the two to four

bit decoder **32a** are well known and the decoder is therefore not described further herein. Flip flops **27** are well known in the art.

The second coarse delay circuit **34** comprises five delay circuits disposed in series with an output drawn from each of the delay circuits to the outputs of the second coarse delay circuit **34**. The delay circuit comprises four delay circuits connected in series to provide a delay of substantially four times that provided by a single delay circuit.

Referring to Fig. 9, a detailed schematic diagram of an alternative fine delay element **28** is shown. A fine delay element of the design shown is suitable for delaying falling edges. A signal provided to the fine delay element **28** is buffered through P1 and N6 and then again through P2 and N7. Poly wire resistors **30** and **31** provide a substantial portion of resistance for an RC circuit. The use of poly wire resistors in series with CMOS inverters improves temperature invariance of the overall resistance as poly wire resistors are less temperature sensitive than intrinsic CMOS buffer output resistance i.e. an inverter without a resistor in series therewith. Resistor values for resistors **30** and **31** are selected to be significantly larger than the intrinsic impedance of the transistors P1, P2, N6, and N7. The buffered signal B is provided to an output buffer comprising four transistors P3, P4, N8, and N9. The buffered signal B is also provided to a source and a drain of each PMOS transistor N0 - N5. Transistor substrates for transistors N0-N5 are electrically connected to V_{DD}. When an appropriate voltage is applied to each gate, a capacitor is formed between the gate oxide and an induced channel of each transistor. The formed capacitors are disposed in parallel. As is well known in the art of electronics, capacitors disposed in parallel are modelled by adding their capacitances together.

The capacitors N0-N5 are each formed of a PMOS transistor having a source and drain shorted together and having a substrate connected to V_{DD}. A gate of each transistor is provided a data signal from the data bus, shown here as D(5:0). The data signals D(5:0) are each electrically coupled to a gate of a transistor. Each transistor N0 - N5, has a different capacitive value. The capacitive value of each transistor is associated with the gate dimensions W and L, therefore varying these dimensions varies the capacitance

between the gate and the channel when formed. A large degree of flexibility is supported when exponentially increasing values in the form of n, 2n, 4n, 8n, 16n, and 32n are selected and where n corresponds to a capacitance required to produce a delay of the desired resolution of the fine delay circuit.

Referring to Fig. 10, a detailed schematic diagram of an alternative fine delay element **28** for delaying both rising and falling edges is shown. A signal provided to the fine delay element **28** is buffered through P1 and N6 and then again through P2 and N7. Poly wire resistors **30** and **31** provide a substantial portion of resistance for an RC circuit. Resistor values for resistors **30** and **31** are selected to be significantly larger than the intrinsic impedance of the transistors P1, P2, N6, and N7. The buffered signal B is provided to an output buffer comprising four transistors P3, P4, N8, and N9. The buffered signal B is also provided to a source and a drain of each PMOS transistor N0 - N2 and a source and a drain of each NMOS transistor N3 - N5. Transistor substrates for transistors N0-N2 are electrically connected to V_{DD}. Transistor substrates for transistors N3-N5 are electrically connected to ground. When an appropriate voltage is applied to each gate, a capacitor is formed between the gate oxide and an induced channel of each transistor. The formed capacitors are disposed in parallel. As is well known in the art of electronics, capacitors disposed in parallel are modelled by adding their capacitances together.

A gate of each transistor is provided a data signal from the data bus, shown here as D(5:0). The data signals D(5:0) are each electrically coupled to a gate of a transistor. Each transistor N0 - N5, has different gate dimensions and, therefore, a different capacitive value. A large degree of flexibility is supported when exponentially increasing values in the form of n, 2n, 4n, 8n, 16n, and 32n are selected and where n corresponds to a capacitance required to produce a delay of the desired resolution of the fine delay circuit. Preferably when delaying rising and falling edges, a greater number of transistors than those shown in the circuit diagram are employed.

Those of skill in the art will recognise that layout considerations are significant in IC design. The above design is no exception. In design of such a circuit, modelling

assumptions are critical to accurate simulation. Layout is accomplished prior to simulation and some layout design rules may require alteration.

In layout of a fine delay element as described above reduces intrinsic capacitance and, by sharing adjacent pads greatly reduces integrated circuit layout space required. Referring to Fig. 10, a prior art layout implementation for a number of transistors is shown. Each transistor is provided with its own source, drain and gate. In such an implementation, the space a transistor occupies is equal to the transistor space plus an additional amount of inter component spacing required. As can be seen in Fig. 10, a small number of transistors occupy a significant amount of integrated circuit space.

Referring to Fig. 12a, a plurality of transistors are shown wherein space between transistors, inter component spacing, is removed and adjacent source or drain pads are shared by two or more transistors. The space savings achieved through such a layout are substantial. Firstly, inter component spacing is reduced to 0. Secondly, the space occupied by the transistors shown is the number of transistors times the space required for a single transistor minus the number of transistors less one times the space occupied by a source or drain. The savings are thus linearly proportional to a number of digitally controlled capacitors laid out in this fashion.

Referring to Fig. 12b, a first transistor source is coupled to the trace B. A transistor drain for that transistor source also acts as a source for a next transistor. This is also coupled to the trace B. In use, a capacitor is formed between a gate and a channel c formed between a source and a drain and shown; the use of a same structure as a source for a first transistor and as a drain for a second transistor results in little effect on capacitance and results in saved board space, less intrinsic capacitance and a lower cost circuit element.

Numerous other embodiments may be envisaged without departing from the scope of the invention as defined by the claims.

Claims

1. A MOS variable delay circuit comprising:

a) a first terminal;

b) a second terminal;

c) a reference voltage terminal;

d) a resistive means coupled in series with the first terminal and the second terminal;

e) a transistor having a source, a gate, a drain, and a substrate, the source and the drain electrically coupled with the second terminal, and the substrate electrically coupled with the reference voltage terminal; and,

f) means for providing to the gate a binary digital signal for selecting between a first capacitance and a second substantially higher capacitance.

2. A MOS variable delay circuit as defined in claim 1 wherein the resistive means comprises a poly resistor.

3. A MOS variable delay circuit as defined in claim 1, further comprising an input buffer comprising a transistor having a gate, a source and a drain, the gate coupled to an input terminal, the source coupled to a reference voltage source, V_{DD}, and the drain coupled to the first terminal.

4. A MOS variable delay circuit as defined in claim 1, wherein the resistive means comprises a poly resistor, the transistor is an NMOS transistor, and the reference voltage terminal is a ground voltage terminal.

5. A MOS variable delay circuit as defined in claim 1, wherein the resistive means comprises a poly resistor, the transistor is a PMOS transistor, and the reference voltage terminal is a V_{DD} voltage terminal.

6. A MOS variable delay circuit as defined in claim 1 further comprising:
g) a second transistor having a second source, a second gate, a second drain, and a second substrate, the second source and the second drain electrically coupled with the second terminal, and the second substrate electrically coupled with the reference voltage terminal; and,
h) means for providing to the second gate a second binary digital signal for selecting between a first capacitance and a second substantially higher capacitance.

7. A MOS variable delay circuit as defined in claim 6 wherein the resistive means comprises a poly resistor.

8. A MOS variable delay circuit as defined in claim 1 further comprising:
g) a plurality of further transistors each having a further source, a gate, a further drain, and a further substrate, each further source and each further drain electrically coupled with the second terminal, and each further substrate electrically coupled with the reference voltage terminal; and,
h) means for providing to each gate of a further transistor a further binary digital signal for selecting between a first capacitance and a second substantially higher capacitance.

9. A MOS variable delay circuit as defined in claim 8 wherein the resistive means comprises a poly resistor.

10. A MOS variable delay circuit as defined in claim 8, further comprising an input buffer comprising a transistor having a gate, a source and a drain, the gate coupled to an input terminal, the source coupled to a reference voltage source, V_{DD}, and the drain coupled to the first terminal.

11. A MOS variable delay circuit as defined in claim 8, wherein the resistive means comprises a poly resistor, the transistors are NMOS transistors, and the reference voltage terminal is a ground voltage terminal.

12. A MOS variable delay circuit for delaying a source signal as defined in claim 8, wherein the resistive means comprises a poly resistor, the transistors are PMOS transistors, and the reference voltage terminal is a V_{DD} voltage terminal.

13. A MOS variable delay circuit as defined in claim 8 wherein one of a source and a drain of a first transistor is a source or a drain of a second other transistor.

14. A MOS variable delay circuit comprising:

a) a first terminal;

b) a second terminal;

c) a first reference voltage terminal;

d) a second reference voltage terminal;

e) a resistive means coupled in series with the first terminal and the second terminal;

f) a plurality of n-type transistors each having a source, a gate, a drain, and a substrate, the source and the drain electrically coupled with the second terminal, and the substrate electrically coupled with the first reference voltage terminal;

g) a plurality of p-type transistors each having a source, a gate, a drain, and a substrate, the source and the drain electrically coupled with the second terminal, and the substrate electrically coupled with the second reference voltage terminal; and,

h) means for providing to each gate a binary digital signal for selecting between a first capacitance and a second substantially higher capacitance.

15. A MOS variable delay circuit as defined in claim 14 wherein the resistive means comprises a poly resistor.

16. A MOS variable delay circuit as defined in claim 14, wherein the first reference voltage terminal is electrically coupled to a ground terminal and the second reference voltage terminal is electrically coupled to a V_{DD} terminal.

17. A MOS variable delay circuit as defined in claim 14 wherein one of a source and a drain from a first transistor of a type selected from n-type or p-type is a source or a drain of a second other transistor having a same type.

18. A fine delay circuit for use in a vernier delay circuit comprising:

a) an input terminal;

b) an input buffer comprising at least a first transistor comprising a first gate coupled with the input terminal, a first source coupled with a voltage terminal V_{DD} and a first drain, and a poly resistor having a first terminal and a second terminal, the first terminal electrically coupled with the first drain;

c) an output terminal electrically coupled to the second terminal of the poly resistor;

d) a first reference voltage terminal,

e) at least a second transistor having a second source, a second gate, a second drain, and a substrate, the second source and the second drain electrically coupled with at least the output terminal, and the substrate electrically coupled with the first reference voltage terminal; and,

f) means for providing to the second gate a binary digital signal for selecting between a first gate-channel capacitance and a second substantially higher gate-channel capacitance.

19. A delay circuit susbstantially as herein described with reference to each of Figs 2 to 12 of the accompanying drawings.

The Patent Office

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Application No: GB 9727375.9 **Examiner:** K. Sylvan
Claims searched: 1-19 **Date of search:** 15 April 1998

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Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.P): H3P (PPMD)

Int Cl (Ed.6): H03K (5/13)

Other:

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	US5416436	France Telecom (Rainard). See the figures.	1,6,8
A	US5180938	Samsung. See the figures.	-

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